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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : Gilbert Wolrich et al. Art Unit: 2177
Serial No.: 10/039,289 Examiner:
Filed : January 4, 2002 Srirama Channavajjala
Assignee : Intel Corporation
Title : QUEUE ARRAYS IN NETWORK DEVICES

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
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Technology Center 2100

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Kindly accept this Information Disclosure Statement under Rule 97(c)(2). The rule 17(p) certification fee of \$180 is enclosed.

The documents are in the English language; hence no concise explanation is necessary per Rule 98(a)(3).

Consideration of the foregoing and enclosures plus the return of a copy of the enclosed form PTO-1449 with the

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Typed or Printed Name of Person Signing Certificate

Applicant : Gilbert Wolrich et al.
Serial No.: 10/039,289
Filed : January 4, 2002


Attorney's Docket No.:10559-612001

Examiner's initials in the left column per MPEP 609 are
earnestly solicited along with an early action on the merits.

Please apply any additional charges or credits to Deposit
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Respectfully submitted,

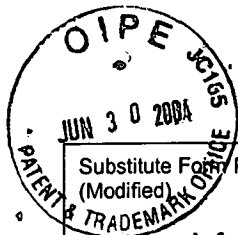
Date: 6/28/04



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Substitute Form PTO-1449 (Modified) Information Disclosure Statement by Applicant (Use several sheets if necessary) (37 CFR §1.98(b))	U.S. Department of Commerce Patent and Trademark Office	Attorney's Docket No. 10559-612001	Application No. 10/039,289
	Applicant Gilbert Wolrich et al.		
	Filing Date 01/04/02	Group Art Unit 2177	JUL 02 2004

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U.S. Patent Documents							
Examiner Initial	Desig. ID	Document Number	Publication Date	Patentee	Class	Subclass	Filing Date If Appropriate
	AA	09/475,614	12/1999	Wolrich, et al.			
	AB	09/473,571	12/1999	Wolrich, et al.			

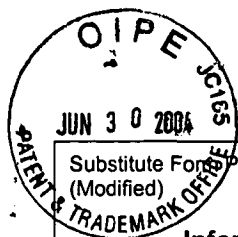
Foreign Patent Documents or Published Foreign Patent Applications								
Examiner Initial	Desig. ID	Document Number	Publication Date	Country or Patent Office	Class	Subclass	Translation	
							Yes	No
	/ AC	WO 01/50679	07/2001	WIPO				
	/ AD	WO 01/50247	07/2001	WIPO				
	/ AE	WO 01/48619	07/2001	WIPO				
	/ AF	WO 01/48606	07/2001	WIPO				
	/ AG	WO 01/48596	07/2001	WIPO				
	/ AH	WO 01/16782	03/2001	WIPO				
	/ AI	WO 01/16770	03/2001	WIPO				
	/ AJ	WO 01/16769	03/2001	WIPO				
	/ AK	WO 01/15718	03/2001	WIPO				
	/ AL	WO 97/38372	10/1997	WIPO				
	/ AM	WO 94/15287	07/1994	WIPO				
	/ AN	EP 0 809 180	11/1997	Europe				
	/ AO	EP 0 745 933	12/1996	Europe				
	/ AP	EP 0 633 678	01/1995	Europe				
	/ AQ	EP 0 464 715	01/1992	Europe				
	/ AR	EP 0 379 709	08/1990	Europe				
	/ AS	59-111533	06/1984	Japan (w/abstract)				X

Other Documents (include Author, Title, Date, and Place of Publication)		
Examiner Initial	Desig. ID	Document
	AT	Byrd et al., "Multithread Processor Architectures," <i>IEEE Spectrum</i> , Vol. 32, No. 8, New York, 1 August 1995, pp. 38-46.
	AU	Doyle et al., <i>Microsoft Press Computer Dictionary</i> , 2 nd ed., Microsoft Press, Redmond, Washington, USA, 1994, p. 326.

Examiner Signature	Date Considered
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EXAMINER: Initials citation considered. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

Substitute Disclosure Form (PTO-1449)

Substitute Form PTO-1449
(Modified)U.S. Department of Commerce
Patent and Trademark OfficeAttorney's Docket No.
10559-612001Application No.
10/039,299

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**Information Disclosure Statement
by Applicant**

(Use several sheets if necessary)

(37 CFR §1.98(b))

Applicant
Gilbert Wolrich et al.

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Filing Date
01/04/02Group Art Unit
2177 Technology Center 2100**Other Documents (include Author, Title, Date, and Place of Publication)**

Examiner Initial	Desig. ID	Document
	AV	Fillo et al., "The M-Machine Multicomputer," IEEE Proceedings of MICRO-28, 1995, pp. 146-156.
	AW	Gomez et al., "Efficient Multithreaded User-Space Transport for Network Computing: Design and Test of the TRAP Protocol," <i>Journal of Parallel and Distributed Computing</i> , Academic Press, Duluth, Minnesota, USA, vol. 40, no. 1, 10 January 1997, pp. 103-117.
	AX	Haug et al., "Reconfigurable hardware as shared resource for parallel threads," IEEE Symposium on FPGAs for Custom Computing Machines, 1998.
	AY	Hauser et al., "Garp: a MIPS processor with a reconfigurable coprocessor," Proceedings of the 5 th Annual IEEE Symposium on Field-Programmable Custom Computing Machines, 1997.
	AZ	Hyde, R., "Overview of Memory Management," <i>Byte</i> , vol. 13, no. 4, 1998, pp. 219-225.
	AAA	Litch et al., "StrongARMing Portable Communications," IEEE Micro, 1998, pp. 48-55.
	ABB	Schmidt et al., "The Performance of Alternative Threading Architectures for Parallel Communication Subsystems," Internet Document, <i>Online!</i> , 13 November 1998.
	ACC	Thistle et al., "A Processor Architecture for Horizon," IEEE, 1998, pp. 35-41.
	ADD	Tremblay et al., "A Three Dimensional Register File for Superscalar Processors," IEEE Proceedings of the 28 th Annual Hawaii International Conference on System Sciences, 1995, pp. 191-201.
	AEE	Trimberger et al., "A time-multiplexed FPGA," Proceedings of the 5 th Annual IEEE Symposium on Field-Programmable Custom Computing Machines," pp. 22-28, 1998.
	AFF	Turner et al., "Design of a High Performance Active Router," Internet Document, <i>Online</i> , pp. 1-20, 18 March 1999.
	AGG	Vibhatavanij et al., "Simultaneous Multithreading-Based Routers," Proceedings of the 2000 International Conference of Parallel Processing, Toronto, Ontario, Canada, 21-24 August 2000, pp. 362-369.
	AHH	Wazlowski et al., "PRSIM-II computer and architecture," IEEE Proceedings, Workshop on FPGAs for Custom Computing Machines, 1993.

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Date Considered

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